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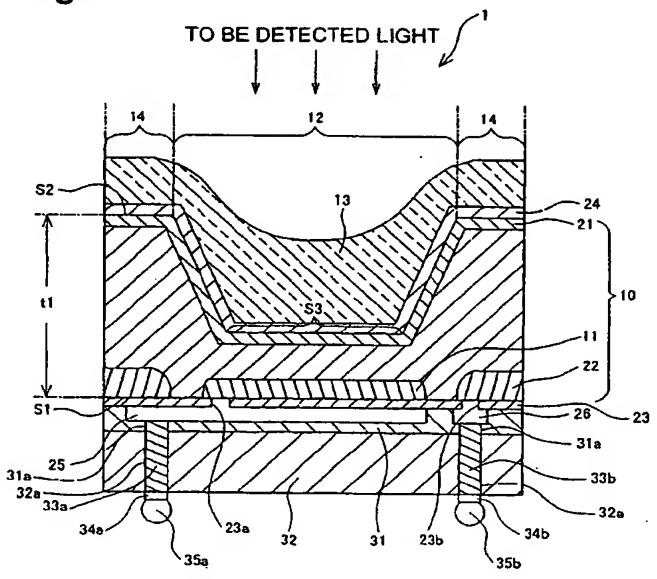
(54) BACKSIDE-ILLUMINATED PHOTODETECTOR

(57) The present invention provides a back illuminated photodetector having a sufficiently small package as well as being capable of suppressing the scattering of to-be-detected light. A back illuminated photodiode 1 comprises an N-type semiconductor substrate 10, a P+-type doped semiconductor region 11, a recessed portion 12, and a coating layer 13. In the surface layer on the upper surface S 1 side of the N-type semiconductor substrate 10 is formed the P+-type doped semiconductor region 11. In the rear surface S2 of the N-type semiconductor substrate 10 and in an area opposite the P+-type doped semiconductor region 11 is formed the recessed portion 12 that functions as an incident part for to-be-detected light. Also, on the rear surface S2 is provided the coating layer 13 for transmitting to-be-detected light that is made incident into the recessed portion 12. The coating layer 13 is here arranged in such a manner that the portion provided on the recessed portion 12 is sunk lower than the portion provided on the outer edge portion 14 of the recessed portion 12.

Fig.1



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EP 1 648 036 A1

Description

Technical Field

[0001] The present invention relates to a back illuminated photodetector.

Background Art

[0002] In such a conventional back illuminated photodiode 100 as shown in FIG 24, in the superficial surface layer of an N-type silicon substrate 101 are formed a P^+-type highly-doped semiconductor region 102 and an N^+-type highly-doped semiconductor region 103. The P^+-type highly-doped semiconductor region 102 and the N^+-type highly-doped semiconductor region 103 are connected, respectively, with an anode electrode 104 and a cathode electrode 105. On the electrodes 104 and 105 are formed bump electrodes 106 made from solder. Also, the N-type silicon substrate 101 is thinned in the portion corresponding to the P^+-type highly-doped semiconductor region 102 from the rear surface side thereof. The thinned portion functions as an incident part for to-be-detected light.

[0003] As shown in FIG 24, the back-illuminated photodiode 100 is packed into a ceramic package 107 by flip-chip bonding. That is, the bump electrodes 106 of the back illuminated photodiode 100 are connected to solder pads 109 provided on a bottom wiring 108 of the ceramic package 107. The bottom wiring 108 is connected to output terminal pins 110 through wire bonding. Also, on the surface of the ceramic package 107 is seam-welded a window frame 111 using brazing material 112. In the window frame 111 is formed an opening at the position corresponding to the thinned portion of the back illuminated photodiode 100, and in the opening is provided a transmissive window member 113 such as kovar glass for transmitting to-be-detected light.

Patent Document 1: Japanese Published Unexamined Patent Application No. H09-219421

Disclosure of the Invention

Problems to be Solved by the Invention

[0004] However, in such an arrangement of using a ceramic package in a back illuminated photodiode as above, there is a problem in that the package becomes larger.

[0005] Meanwhile, in Patent Document 1 is disclosed a CSP (Chip Size Package) technique for semiconductor electronic components. This technique is adapted to seal the both surfaces of a wafer with semiconductor electronic components built therein using organic material such as resin, and then to form an opening in the organic material provided on one surface side of the wafer by photolithography to form electrodes therein.

[0006] However, trying to apply such a CSP technique to a back illuminated photodiode to reduce the package size leads to the following problem. That is, the back illuminated photodiode is thinned at the portion that functions as an incident part for to-be-detected light, which reduces the mechanical strength thereof. Therefore, not a pyramid collet but a flat collet is used when assembling the back illuminated photodiode. For example, when heating and pressurizing a bump electrode, etc., provided on the surface side of a photodiode, heat and pressure is added from a heater block while the back illuminated photodiode sticks thereto using a flat collet to employ the rear surface thereof as a sticking surface.

[0007] In the case of using a flat collet for a back illuminated photodiode with the rear surface being sealed with resin, the resin may be damaged due to contact with the collet. If the resin in the thinned portion (i.e. incident part for to-be-detected light) of the back illuminated photodiode may thus be damaged, there is a problem in that the damage scatters to-be-detected light. Then, the scattering of to-be-detected light also leads to a reduction in the sensitivity of the back illuminated photodiode.

[0008] The present invention has been made to solve the above-described problems, and an object thereof is to provide a back illuminated photodetector having a sufficiently small package as well as being capable of suppressing the scattering of to-be-detected light.

Means for Solving the Problems

[0009] In order to solve the above-described problem, the present invention is directed to a back illuminated photodetector comprising: a first conductive type semiconductor substrate; a second conductive type doped semiconductor region provided in the first superficial surface layer of the semiconductor substrate; a recessed portion for incidence of to-be-detected light formed in the second surface of the semiconductor substrate and in an area opposite the doped semiconductor region; and a coating layer made of resin for transmitting the to-be-detected light, the coating layer being provided on the second surface, and the coating layer being arranged in such a manner that the portion provided on the recessed portion in the second surface is sunk lower than the portion provided on the outer edge portion of the recessed portion.

[0010] In the back illuminated photodetector, since there is provided the coating layer, the mechanical strength of the back illuminated photodetector can be increased. The increase in mechanical strength allows for dicing at a wafer level, whereby it is possible to obtain a chip-sized back illuminated photodetector. Accordingly, it is possible to achieve a back illuminated photodetector having a sufficiently small package. The coating layer is also made of resin for transmitting to-be-detected light not only to increase the mechanical strength of the back illuminated photodetector, but also to function as a transmissive window member for to-be-detected light.

[0011] Further, the coating layer is arranged in such a

manner that the portion provided on the recessed portion is sunk lower than the portion provided on the outer edge portion of the recessed portion. Therefore, even if a flat collet may be used in an assembling operation, the surface of the coating layer provided on the recessed portion is not brought into contact with the flat collet. Thus, the incident part for to-be-detected light within the surface of the coating layer cannot be damaged, whereby it is possible to suppress the scattering of to-be-detected light.

[0012] The back illuminated photodetector according to the present invention preferably comprises a supporting film provided on the first surface of the semiconductor substrate to support the semiconductor substrate. In this case, the mechanical strength of the back illuminated photodetector can be increased.

[0013] Further, the back illuminated photodetector preferably comprises a filling electrode penetrating through the supporting film and connected electrically to the doped layer at one end thereof. In this case, it is possible to take a detected signal easily outside the back illuminated photodetector.

[0014] It is preferable that a highly-doped semiconductor region with impurities of the first conductive type added thereto at a high concentration is exposed across the entire side surface of the semiconductor substrate. In this case, even if a side surface of the semiconductor substrate may be damaged through dicing, etc., the highly-doped semiconductor region can trap unnecessary carriers that are generated in the vicinity of the side surface of the semiconductor substrate, and therefore can suppress dark current and/or noise.

[0015] It is preferred that a highly-doped semiconductor layer with impurities of the first conductive type added thereto at a high concentration is provided in the bottom portion of the recessed portion within the second superficial surface layer of the semiconductor substrate. The highly-doped semiconductor layer functions as an accumulation layer. This can make carriers generated upon incidence of to-be-detected light easy to move toward the first surface of the semiconductor substrate, resulting in an increase in the sensitivity of the back illuminated photodetector.

[0016] It is preferable that a highly-doped semiconductor layer with impurities of the first conductive type added thereto at a high concentration is provided in the second superficial surface layer in the outer edge portion of the semiconductor substrate. In this case, even if there may be crystal defects in the vicinity of the second superficial surface in the outer edge portion, the highly-doped semiconductor layer can suppress dark current and/or noise due to the crystal defects.

Effects of the Invention

[0017] In accordance with the present invention, it is possible to achieve a back illuminated photodetector having a sufficiently small package as well as being capable of suppressing the scattering of to-be-detected light.

Brief Description of the Drawings

[0018] FIG. 1 is a cross-sectional view showing a first embodiment of a back illuminated photodetector according to the present invention.

FIG. 2 is a view illustrating the effect of the back illuminated photodiode 1 shown in FIG. 1.

FIG. 3 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 4 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 5 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 6 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 7 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 8 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 9 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 10 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 11 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 12 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 13 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 14 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 15 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 16 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 17 is a step chart showing a method for manufacturing the back illuminated photodiode 1 shown in FIG. 1.

FIG. 18 is a cross-sectional view showing a second embodiment of a back illuminated photodetector according to the present invention.

FIG. 19 is a view illustrating an exemplary method for forming the N^+-type highly-doped semiconductor

region 28 shown in FIG. 18.

FIG. 20 is a view illustrating an exemplary method for forming the N^+-type highly-doped semiconductor region 28 shown in FIG. 18.

FIG. 21 is a view illustrating an exemplary method for forming the N^+-type highly-doped semiconductor region 28 shown in FIG. 18.

FIG. 22 is a plan view showing a third embodiment of a back illuminated photodetector according to the present invention.

FIG. 23 is a cross-sectional view of the back illuminated photodiode array 3 shown in FIG. 22 along the line XII-XII.

FIG. 24 is a cross-sectional view of a conventional back illuminated photodiode.

Description of Symbols

[0019] 1 and 2: Back illuminated photodiodes, 3: Back illuminated photodiode array, 10 and 50: N-type semiconductor substrates, 11 and 51: P^+-type doped semiconductor regions, 12 and 52: Recessed portions, 13 and 53: Coating layers, 14 and 54: Outer edge portions, 20: Semiconductor substrate, 21 and 61: N^+-type highly-doped semiconductor layers, 22; 28 and 62: N^+-type highly-doped semiconductor regions, 23; 24; 63 and 64: Insulating films, 25 and 65: Anode electrodes, 26 and 66: Cathode electrodes, 31 and 71: Passivation films, 32 and 72: Supporting films, 33a; 33b; 73a and 73b: Filling electrodes, 34a; 34b; 74a and 74b: UBMs, 35a; 35b; 75a and 75b: Bumps, S1: Upper surface, S2: Rear surface, S3: Bottom surface of recessed portion, S4: Side surface of the semiconductor substrate 20

Best Modes for Carrying Out the Invention

[0020] Preferred embodiments of a back illuminated photodetector according to the present invention will hereinafter be described in detail with reference to the accompanying drawings. Additionally, in the descriptions of the drawings, identical components are designated by the same reference numerals to omit overlapped description. Also, the dimensional ratios in the drawings do not necessarily correspond to those in the descriptions.

[0021] FIG. 1 is a cross-sectional view showing a first embodiment of a back illuminated photodetector according to the present invention. The back illuminated photodiode 1 is adapted to receive to-be-detected light from the rear surface thereof, to generate carriers upon incidence of the to-be-detected light, and then to output the generated carriers as a detected signal from the upper surface thereof. The back illuminated photodiode 1 comprises an N-type semiconductor substrate 10, a P^+-type doped semiconductor region 11, a recessed portion 12, and a coating layer 13. As the N-type semiconductor substrate 10, for example, a silicon substrate with N-type impurities such as phosphorous added thereto can be used. The impurity concentration of the N-type semiconductor substrate 10 is 10^{12} to $10^{15}/cm^3$, for example. Also, the thickness t1 of the N-type semiconductor substrate 10 is 200μm to 500μm, for example.

[0022] In the surface layer on the upper surface (first surface) S1 side of the N-type semiconductor substrate 10 is partially formed the P^+-type doped semiconductor region 11. The P^+-type doped semiconductor region 11 is provided with P-type impurities such as boron to form a PN junction with the N-type semiconductor substrate 10. The impurity concentration of the P^+-type doped semiconductor region 11 is 10^{15} to $10^{20}/cm^3$, for example. Also, the depth of the P^+-type doped semiconductor region 11 is 0.1μm to 20μm, for example.

[0023] In the rear surface (second surface) S2 of the N-type semiconductor substrate 10 and in an area opposite the P^+-type doped semiconductor region 11 is formed the recessed portion 12. The recessed portion 12 functions as an incident part for to-be-detected light. The recessed portion 12 has a shape that narrows gradually from the rear surface S2 to the upper surface S1. More specifically, the recessed portion 12 may have, for example, a square pyramid shape or a tapered shape that narrows gradually from the rear surface S2 to the upper surface S1. The depth of the recessed portion 12 is 2μm to 400μm, for example. Also, due to the thus formed recessed portion 12, the area between the bottom surface S3 of the recessed portion and the P^+-type doped semiconductor region 11 within the N-type semiconductor substrate 10 is made thinner than the other areas so that carriers generated upon incidence of to-be-detected light via the rear surface S2 can easily reach near the P^+-type doped semiconductor region 11 provided in the surface layer on the upper surface S1 side. In addition, the thickness of the thinned area is 10μm to 200μm, for example.

[0024] On the rear surface S2 of the N-type semiconductor substrate 10 is provided the coating layer 13. The coating layer 13 is made of resin transparent to to-be-detected light, that is, having a sufficient transmissivity for the wavelength of to-be-detected light. As such resin epoxy-based, silicon-based, acryl-based or polyimide-based one, or composite material thereof can be cited. The coating layer 13 functions as a protective layer for protecting the rear surface S2 as well as a transmissive window member for transmitting to-be-detected light that is made incident into the recessed portion 12. Also, the coating layer 13 is arranged in such a manner that the portion provided on the recessed portion 12 is sunk lower than the portion provided on the outer edge portion 14 of the recessed portion 12. That is, the surface of the coating layer 13 provided in the portion where the recessed portion 12 is formed gets into the N-type semiconductor substrate 10 side deeper than the surface of the coating layer 13 provided in the outer edge portion 14 of the recessed portion 12. Herein, the outer edge portion 14 indicates the portion laterally surrounding the recessed portion 12 within the N-type semiconductor substrate 10. The thickness of the coating layer 13 on

the outer edge portion 14 is 5μm to 500μm, for example, and preferably 250μm.

[0025] The back illuminated photodiode 1 also comprises an N^+-type highly-doped semiconductor layer 21, an N^+-type highly-doped semiconductor region 22, insulating films 23 and 24, an anode electrode 25, and a cathode electrode 26. The N^+-type highly-doped semiconductor layer 21 is formed in the entire surface layer on the rear surface S2 side of the N-type semiconductor substrate 10. The N^+-type highly-doped semiconductor layer 21 is provided with N-type impurities at a concentration higher than in the N-type semiconductor substrate 10. The impurity concentration of the N^+-type highly-doped semiconductor layer 21 is 10^{15} to $10^{20}/cm^3$, for example. Also, the depth of the N^+-type highly-doped semiconductor layer 21 is 0.1μm to 20μm, for example.

[0026] The N^+-type highly-doped semiconductor region 22 is formed in the surface layer on the upper surface S1 side of the N-type semiconductor substrate 10 at a predetermined distance from the P^+-type doped semiconductor region 11. The N^+-type highly-doped semiconductor region 22 is also provided with N-type impurities at a high concentration, as is the case with the N^+-type highly-doped semiconductor layer 21, to be a contact layer for the cathode electrode 26 to be described hereinafter as well as to have a function of suppressing surface leakage current in the upper surface S1. The impurity concentration of the N^+-type highly-doped semiconductor region 22 is 10^{15} to $10^{20}/cm^3$, for example. Also, the depth of the N^+-type highly-doped semiconductor region 22 is 0.1μm to 30μm, for example.

[0027] The insulating films 23 and 24 are formed, respectively, on the upper surface S 1 and the rear surface S2 of the N-type semiconductor substrate 10. The insulating films 23 and 24 are made of SiO_2, for example. The thickness of the insulating film 23 is 0.1μm to 2μm, for example. Meanwhile, the thickness of the insulating film 24 is 0.05μm to 1μm, for example. Also, in the insulating film 23 are formed openings (contact holes) 23a and 23b, one opening 23a being provided within the range of the P^+-type doped semiconductor region 11, while the other opening 23b being provided within the range of the N^+-type highly-doped semiconductor region 22.

[0028] On the insulating film 23 and in the areas including the openings 23a and 23b are formed, respectively, the anode electrode 25 and the cathode electrode 26. The thickness of the electrodes 25 and 26 is 1μm, for example. The electrodes 25 and 26 are provided in such a manner as to fill the respective openings 23a and 23b. Thus, the anode electrode 25 is connected directly to the P^+-type doped semiconductor region 11 through the opening 23a, while the cathode electrode 26 is connected directly to the N^+-type highly-doped semiconductor region 22 through the opening 23b. As the anode and cathode electrodes 25 and 26, for example, Al, can be used.

[0029] The back illuminated photodiode 1 further comprises a passivation film 31, a supporting film 32, filling electrodes 33a and 33b, UBMs (Under Bump Metals) 34a and 34b, and bumps 35a and 35b. The passivation film 31 is provided on the upper surface S1 of the N-type semiconductor substrate 10 in such a manner as to cover the insulating film 23, anode electrode 25, and cathode electrode 26. Also, in the portions provided on the anode electrode 25 and the cathode electrode 26 within the passivation film 31 are formed through holes 31a to be filled with the filling electrodes 33a and 33b to be described hereinafter. The passivation film 31 is made of SiN, for example, to protect the upper surface S1 of the N-type semiconductor substrate 10. The passivation film 31 can be formed by, for example, a plasma-CVD method. Also, the thickness of the passivation film 31 is 1μm, for example.

[0030] On the passivation film 31 is formed the supporting film 32. The supporting film 32 is adapted to support the N-type semiconductor substrate 10. Also, in the portions corresponding to the through holes 31a in the passivation film 31 within the supporting film 32 are formed through holes 32a to be filled with the filling electrodes 33a and 33b that also fill the through holes 31a. As a material of the supporting film 32, for example, resin or SiO_2, etc., that can be formed by, for example, a plasma-CVD method can be used. Also, the thickness of the supporting film 32 is 2μm to 100μm, for example, and preferably about 50μm.

[0031] The filling electrodes 33a and 33b fill the through holes 31a and 32a, and are brought into contact, respectively, with the anode electrode 25 and the cathode electrode 26 at one end thereof to be connected electrically to the P^+-type doped semiconductor region 11 and the N^+-type highly-doped semiconductor region 22. Also, the other end of the filling electrodes 33a and 33b is exposed at the surface of the supporting film 32. That is, the filling electrodes 33a and 33b penetrate through the passivation film 31 and the supporting film 32 to extend, respectively, from the anode electrode 25 and the cathode electrode 26 to the surface of the supporting film 32. In addition, the filling electrodes 33a and 33b each have an approximately cylindrical shape. The filling electrodes 33a and 33b are adapted to connect, respectively, the electrodes 25 and 26 and the bumps 35a and 35b to be described hereinafter electrically with each other. The filling electrodes 33a and 33b are made of Cu, for example. Also, the diameter of the through holes 31a and 32a is 10μm to 200μm, for example, and preferably about 100μm.

[0032] On the exposed portions of the filling electrodes 33a and 33b at the surface of the supporting film 32 are formed the UBMs 34a and 34b. The UBMs 34a and 34b are composed of accumulation films made ofNi and Au, for example. Also, the thickness of the UBMs 34a and 34b is 0.1μm to 5μm, for example.

[0033] On the surfaces of the UBMs 34a and 34b on the opposite side of the filling electrodes 33a and 33b are formed the bumps 35a and 35b. The bumps 35a and

35b are therefore connected, respectively, to the anode electrode 25 and the cathode electrode 26 electrically. The bumps 35a and 35b each have an approximately spherical shape except for the surfaces in contact with the UBMs 34a and 34b. As the bumps 35a and 35b, for example, solder, gold, Ni-Au, Cu, or resin containing metal filler can be used.

[0034] The operation of the back illuminated photodiode 1 will here be described. It is assumed here that the back illuminated photodiode 1 is applied with a reverse bias voltage, and that there is generated a depletion layer in the thinned area in the N-type semiconductor substrate 10. When to-be-detected light penetrates through the coating layer 13 and then enters the N-type semiconductor substrate 10 from the recessed portion 12, the light is absorbed mainly in the thinned area. Accordingly, in the area, carriers (holes and electrons) are generated. The generated holes and electrons are moved, respectively, to the P^+-type doped semiconductor region 11 and the N^+-type highly-doped semiconductor region 22 in accordance with the reverse bias electric field. Holes and electrons that have reached the P^+-type doped semiconductor region 11 and the N^+-type highly-doped semiconductor region 22 are moved to the bumps 35a and 35b from the filling electrodes 33a and 33b and the UBMs 34a and 34b to be output as a detected signal from the bumps 35a and 35b.

[0035] The effect of the back illuminated photodiode 1 will here be described. In the back illuminated photodiode 1, since there is provided the coating layer 13, the mechanical strength of the back illuminated photodiode 1 is increased. In particular, since the coating layer 13 is provided on the recessed portion 12, it is possible to prevent the thinned area in the N-type semiconductor substrate 10 from being distorted, flexed or damaged even if pressure and/or heat may be applied to the back illuminated photodiode 1 in an assembling operation. Also, the increase in mechanical strength allows for dicing at a wafer level, whereby it is possible to obtain a chip-sized back illuminated photodiode 1. Accordingly, there is achieved a back illuminated photodiode 1 having a sufficiently small package. In addition, since there is no need for a ceramic package, etc., it is possible to reduce the cost of manufacturing a back illuminated photodiode 1. There is thus achieved an inexpensive and highly reliable as well as a small back illuminated photodiode 1.

[0036] Further, the coating layer 13 is arranged in such a manner that the portion provided on the recessed portion 12 is sunk lower than the portion provided on the outer edge portion 14 of the recessed portion 12. Therefore, even if a flat collet FC may be used in an assembling operation as shown in FIG. 2, the surface of the coating layer 13 provided on the recessed portion 12 is not brought into contact with the flat collet FC. Thus, the incident part for to-be-detected light within the surface of the coating layer 13 cannot be damaged, whereby it is possible to suppress the scattering of to-be-detected light. Thus, a highly sensitive back illuminated photodiode 1 is achieved.

[0037] In addition, providing the coating layer 13 also on the outer edge portion 14 prevents the flat collet FC from being brought into direct contact with the outer edge portion 14. It is thus possible to prevent the generation of crystal defects in the outer edge portion 14 due to contact with the flat collet FC, and therefore to suppress dark current and/or noise due to the crystal defects.

[0038] Also, as the coating layer 13 resin is used, which makes it easy to form the coating layer 13 into a desired shape.

[0039] The provided supporting film 32 further increases the mechanical strength of the back illuminated photodiode 1.

[0040] The provided filling electrodes 33a and 33b make it easy to take a detected signal outside from the electrodes 25 and 26. Additionally, the filling electrodes 33a and 33b may be formed on the sidewalls of the through holes 31a and 32a to be connected electrically to the anode electrode 25 and the cathode electrode 26.

[0041] The N^+-type highly-doped semiconductor layer 21 is formed in the entire surface layer on the rear surface S2 side of the N-type semiconductor substrate 10. The N^+-type highly-doped semiconductor layer 21 provided in the bottom surface S3 of the recessed portion 12 within the surface layer of the rear surface S2 functions as an accumulation layer. This can prevent carriers generated in the N-type semiconductor substrate 10 from being recombined in the vicinity of the bottom surface S3. Thus, a more highly sensitive back illuminated photodiode 1 is achieved. Here, the impurity concentration of the N^+-type highly-doped semiconductor layer 21 is preferably $10^{15}/cm^3$ or more. In this case, the N^+-type highly-doped semiconductor layer 21 can suitably function as an accumulation layer.

[0042] Also, even if there may be crystal defects in the outer edge portion 14, the N^+-type highly-doped semiconductor layer 21, which is provided in the surface layer on the rear surface S2 side within the outer edge portion 14 of the N-type semiconductor substrate 10, can suppress dark current and/or noise due to the crystal defects. Therefore, in accordance with the back illuminated photodiode 1, it is possible to obtain a detected signal at a high S/N ratio. Also, here, the impurity concentration of the N^+-type highly-doped semiconductor layer 21 is preferably $10^{15}/cm^3$ or more. In this case, the N^+-type highly-doped semiconductor layer 21 can suppress dark current and/or noise due to crystal defects sufficiently.

[0043] An exemplary method for manufacturing the back illuminated photodiode 1 shown in FIG. 1 will here be described with reference to FIG. 3 to FIG. 17. First, there is prepared an N-type semiconductor substrate 10 made of an N-type silicon wafer with the upper surface S 1 and the rear surface S2 thereof being formed into (100) planes. The N-type semiconductor substrate 10 is thermally oxidized to form an insulating film made of SiO_2 on the upper surface S 1 of the N-type semiconductor substrate 10. Also, in predetermined portions of the in-

sulating film are formed openings, and then phosphorous is doped into the N-type semiconductor substrate 10 from the openings to form N^+-type highly-doped semiconductor regions 22. Subsequently, the N-type semiconductor substrate 10 is oxidized to form an insulating film on the upper surface S1. Similarly, in predetermined portions of the insulating film are formed openings, and then boron is doped into the N-type semiconductor substrate 10 from the openings to form P^+-type doped semiconductor regions 11. Subsequently, the N-type semiconductor substrate 10 is oxidized to form an insulating film 23 on the upper surface S1 (FIG. 3).

[0044] Next, the rear surface S2 of the N-type semiconductor substrate 10 is polished, and SiN 82 is deposited on the rear surface S2 of the N-type semiconductor substrate 10 by LP-CVD (FIG. 4). Also, in the SiN 82 on the rear surface S2 are formed openings 85 to form recessed portions 12 (FIG. 5). Then, an etching operation is performed using KOH, etc., through the openings 85 to form recessed portions 12 (FIG. 6).

[0045] Next, after the SiN 82 is removed, ion implantation, etc., is performed onto the rear surface S2 side of the N-type semiconductor substrate 10 with the recessed portions 12 formed therein to dope N-type impurities and thereby to form an N^+-type highly-doped semiconductor layer 21 in the entire surface layer on the rear surface S2 side (FIG. 7). Then, the substrate is thermally oxidized to form an insulating film 24 in the entire surface layer on the rear surface S2 side (FIG. 8). Contact holes for electrodes are formed in the insulating film 23 on the upper surface S1, and after aluminum is deposited on the upper surface S1, a predetermined pattern is made to form anode electrodes 25 and cathode electrodes 26 (FIG. 9).

[0046] Next, a passivation film 31 made of SiN is deposited on the upper surface S1 of the N-type semiconductor substrate 10, on which the anode electrodes 25 and the cathode electrodes 26 are formed, by a plasma-CVD method. Also, openings 31a are formed in portions corresponding to bumps 35a and 35b within the passivation film 31 (FIG. 10). Further, a thick supporting film 32 made of resin is formed on the upper surface S1, and openings 32a are formed in the portions corresponding to the openings 31 a in the passivation film 31. Here, as the supporting film 32, resin such as epoxy-based, acryl-based or polyimide-based one can be used. Alternatively, SiO_2 formed by plasma-CVD, etc., may be used. Also, the openings 32a in the supporting film 32 can be formed by a photolithography method using, for example, photosensitive resin or by a patterning process such as etching (FIG. 11). In addition, a conductive material 33 made of Cu is deposited in such a manner as to fill the openings 31a and 32a. This can be made through the steps of, for example, depositing a Cu seed layer, etc., by sputtering, etc., on the surface of the anode electrodes 25 and the cathode electrodes 26 that are exposed from the openings 31a and 32a, and depositing Cu, etc., by plating on the Cu seed layer (FIG. 12).

[0047] Next, the surface of the conductive material 33 is polished to remove the conductive material 33 deposited on the supporting film 32. Thus, filling electrodes 33a and 33b are formed (FIG. 13). Also, after a coating layer 13 made of resin is applied by spin coating or printing, etc., in such a manner as to fully cover the rear surface S2, the applied coating layer 13 is hardened. Here, the portion of the coating layer 13 provided on the recessed portion 12 is to be sunk (FIG. 14). Further, UBMs 34a and 34b composed of accumulation films made of Ni and Au, etc., are formed on the filling electrodes 33a and 33b on the upper surface S1 by electroless plating. In addition, bumps 35a and 35b made of solder, etc., are formed on the UBMs 34a and 34b by printing or a ball-mounting method, etc., (FIG. 15).

[0048] Finally, in order to obtain individually separated back illuminated photodiodes 1, dicing is performed. As indicated by the alternate long and short dashed lines L1 in FIG. 16, the N-type semiconductor substrate 10 is diced at the center of each outer edge portion 14 on the rear surface S2 side. Thus, a back illuminated photodiode 1 (FIG. 17) is obtained.

[0049] FIG. 18 is a cross-sectional view showing a second embodiment of a back illuminated photodetector according to the present invention. The back illuminated photodiode 2 comprises a semiconductor substrate 20, a P^+-type doped semiconductor region 11, a recessed portion 12, and a coating layer 13.

[0050] In the surface layer on the upper surface S 1 side of the semiconductor substrate 20 is partially formed the P^+-type doped semiconductor region 11. Meanwhile, in the rear surface S2 of the semiconductor substrate 20 and in an area opposite the P^+-type doped semiconductor region 11 is formed the recessed portion 12. Also, on the rear surface S2 of the semiconductor substrate 20 is provided the coating layer 13. The coating layer 13 is arranged in such a manner that the portion provided on the recessed portion 12 is sunk lower than the portion provided on the outer edge portion 14 of the recessed portion 12.

[0051] The back illuminated photodiode 2 also comprises an N^+-type highly-doped semiconductor region 28, insulating films 23 and 24, an anode electrode 25, and a cathode electrode 26. The N^+-type highly-doped semiconductor region 28 is formed in such a manner as to be exposed at the entire side surfaces S4 of the semiconductor substrate 20. The N^+-type highly-doped semiconductor region 28 also reaches the entire rear surface S2 of the semiconductor substrate 20. Therefore, the portion 20a within the semiconductor substrate 20, in which neither the P^+-type doped semiconductor region 11 nor the N^+-type highly-doped semiconductor region 28 is formed, is surrounded entirely by the N^+-type highly-doped semiconductor region 28 from the side surface S4 sides and the rear surface S2 side of the semiconductor substrate 20.

[0052] An exemplary method for forming the N^+-type highly-doped semiconductor region 28 will here be described with reference to FIG. 19 to FIG. 21. First, there

is prepared a semiconductor substrate 20. In the semiconductor substrate 20, an N^+-type highly-doped semiconductor layer 41 is diffused from the rear surface S2 with a part on the upper surface S1 side remaining. The remaining part on the upper surface S1 side is an N-type doped semiconductor layer 42 having an impurity concentration lower than that of the N^+-type highly-doped semiconductor layer 41 (FIG. 19). Next, N-type impurities are doped at a high concentration from the upper surface S1 side to form N^+-type highly-doped semiconductor regions 43 (FIG. 20). Then, the N-type impurities are diffused further deeply by heat treatment so that the N^+-type highly-doped semiconductor regions 43 reach the N^+-type highly-doped semiconductor layer 41 (FIG. 21). There is thus formed an N^+-type highly-doped semiconductor region 28 composed of the N^+-type highly-doped semiconductor layer 41 and the N^+-type highly-doped semiconductor regions 43. Additionally, in FIG. 21, the areas where a P^+-type doped semiconductor region 11 and a recessed portion 12 are to be formed are indicated, respectively, by the dashed lines L2 and L3. In accordance with the method, since it is possible to omit the step of doping impurities from the rear surface S2 side of the semiconductor substrate 20, the manufacturing process for the N^+-type highly-doped semiconductor region 28 and therefore for the entire back illuminated photodiode 2 is simplified.

[0053] Returning to FIG. 18, on the upper surface S1 and the rear surface S2 of the semiconductor substrate 20 are formed, respectively, the insulating films 23 and 24. Also, in the insulating film 23 are formed openings 23a and 23b, one opening 23a being provided within the range of the P^+-type doped semiconductor region 11, while the other opening 23b being provided within the range of the N^+-type highly-doped semiconductor region 28.

[0054] On the insulating film 23 and in the areas including the openings 23a and 23b are formed, respectively, the anode electrode 25 and the cathode electrode 26. The electrodes 25 and 26 are provided in such a manner as to fill the respective openings 23a and 23b. Thus, the anode electrode 25 is connected directly to the P^+-type doped semiconductor region 11 through the opening 23a, while the cathode electrode 26 is connected directly to the N^+-type highly-doped semiconductor region 28 through the opening 23b.

[0055] The back illuminated photodiode 2 further comprises a passivation film 31, a supporting film 32, filling electrodes 33a and 33b, UBMs 34a and 34b, and bumps 35a and 35b. The passivation film 31 is provided on the upper surface S1 of the semiconductor substrate 20 in such a manner as to cover the insulating film 23, anode electrode 25, and cathode electrode 26. On the passivation film 31 is formed the supporting film 32. Also, the filling electrodes 33a and 33b penetrate through the passivation film 31 and the supporting film 32 to extend, respectively, from the anode electrode 25 and the cathode electrode 26 to the surface of the supporting film 32. On the exposed portions of the filling electrodes 33a and 33b at the surface of the supporting film 32 are formed the UBMs 34a and 34b. On the surfaces of the UBMs 34a and 34b on the opposite side of the filling electrodes 33a and 33b are formed the bumps 35a and 35b.

[0056] The effect of the back illuminated photodiode 2 will here be described. In the back illuminated photodiode 2, since there is provided the coating layer 13, the mechanical strength of the back illuminated photodiode 2 is increased. Also, the increase in mechanical strength allows for dicing at a wafer level, whereby it is possible to obtain a chip-sized back illuminated photodiode 2. Accordingly, there is achieved a back illuminated photodiode 2 having a sufficiently small package.

[0057] Further, the coating layer 13 is arranged in such a manner that the portion provided on the recessed portion 12 is sunk lower than the portion provided on the outer edge portion 14 of the recessed portion 12. Therefore, even if a flat collet may be used in an assembling operation, the surface of the coating layer 13 provided on the recessed portion 12 is not brought into contact with the flat collet. Thus, the incident part for to-be-detected light within the surface of the coating layer 13 cannot be damaged, whereby it is possible to suppress the scattering of to-be-detected light. Thus, a highly sensitive back illuminated photodiode 2 is achieved.

[0058] Also, in the back illuminated photodiode 2, the N^+-type highly-doped semiconductor region 28 is formed in such a manner as to be exposed at the entire side surfaces S4 of the semiconductor substrate 20. Thus, the N^+-type highly-doped semiconductor region 28 can trap unnecessary carriers that are generated in the vicinity of the side surfaces S4 of the semiconductor substrate 20 and thereby can suppress dark current and/or noise. Although the side surfaces S4 correspond to dicing lines whereby there is a possibility of causing crystal defects in dicing, the N^+-type highly-doped semiconductor region 28 can also suppress dark current and/or noise due to the crystal defects. Therefore, in accordance with the back illuminated photodiode 2, it is possible to obtain a detected signal at a higher S/N ratio.

[0059] In addition, the portion 20a within the semiconductor substrate 20 is surrounded entirely by the N^+-type highly-doped semiconductor region 28 from the side surface S4 sides and the rear surface S2 side of the semiconductor substrate 20. Thus, a PIN structure in which the surrounded portion 20a is employed as an I-layer is achieved. The back illuminated photodiode 2 can be provided with a higher voltage and thereby can increase the width of the depletion layer due to such a PIN structure, which can increase the sensitivity as well as reduce the capacity thereof to achieve a high-speed response.

[0060] FIG. 22 is a plan view showing a third embodiment of a back illuminated photodetector according to the present invention. The back illuminated photodiode array 3 is composed of a total of sixty-four back illuminated photodiodes that are arranged in an eight-by-eight grid pattern. The arrangement pitch of these photodiodes

is 1mm, for example. FIG. 22 shows the appearance of the back illuminated photodiode array 3 when viewed from the rear surface side. The rear surface of each photodiode is covered with a coating layer, and is formed in such a manner that predetermined portions of the coating layer are sunk, as is the case with the back illuminated photodiode 1 shown in FIG. 1. In FIG. 22, the sunk portions of the coating layer are indicated by the dashed lines L4.

[0061] FIG. 23 is a cross-sectional view of the back illuminated photodiode array 3 shown in FIG 22 along the line XII-XII. In the cross-sectional view are shown two photodiodes P1 and P2 among the sixty-four photodiodes shown in FIG. 22. As shown in FIG. 23, the back illuminated photodiode array 3 comprises an N-type semiconductor substrate 50, a P^+-type doped semiconductor region 51, a recessed portion 52, and a coating layer 53.

[0062] In the surface layer on the upper surface S1 side of the N-type semiconductor substrate 50 are formed a plurality of the P^+-type doped semiconductor regions 51. The P^+-type doped semiconductor regions 51 are provided, respectively, for the photodiodes P1 and P2. The area of each P^+-type doped semiconductor region 51 is $0.75 \times 0.75 mm^2$, for example. In the rear surface S2 of the N-type semiconductor substrate 50 and in an area opposite the P^+-type doped semiconductor region 51 is formed the recessed portion 52. Here is formed a plurality of the recessed portions 52 being provided with a plurality of the P^+-type doped semiconductor regions 51. In each of the photodiodes P1 and P2 are provided a pair of a P^+-type doped semiconductor region 51 and a recessed portion 52. Also, on the rear surface S2 of the N-type semiconductor substrate 50 is provided the coating layer 53. The coating layer 53 is arranged in such a manner that the portion provided on the recessed portion 52 is sunk lower than the portion provided on the outer edge portion 54 of the recessed portion 52.

[0063] The back illuminated photodiode array 3 also comprises an N^+-type highly-doped semiconductor layer 61, N^+-type highly-doped semiconductor regions 62, insulating films 63 and 64, anode electrodes 65, and cathode electrodes 66. The N^+-type highly-doped semiconductor layer 61 is formed in the entire surface layer on the rear surface S2 side of the N-type semiconductor substrate 50. The N^+-type highly-doped semiconductor regions 62 are formed in the surface layer on the upper surface S1 side of the N-type semiconductor substrate 50. The N^+-type highly-doped semiconductor regions 62 are preferably provided in such a manner as to surround the P^+-type doped semiconductor regions 51 constituting the respective photodiodes.

[0064] On the upper surface S1 and the rear surface S2 of the N-type semiconductor substrate 50 are formed, respectively, the insulating films 63 and 64. In the insulating film 63 are formed openings 63a and 63b, some openings 63a being provided within the range of the P^+-type doped semiconductor regions 51, while the other openings 63b being provided within the range of the N^+-type highly-doped semiconductor regions 62.

[0065] On the insulating film 63 and in the areas including the openings 63a and 63b are formed, respectively, the anode electrodes 65 and the cathode electrodes 66. In each of the photodiodes P1 and P2 are provided a pair of an anode electrode 65 and a cathode electrode 66. The electrodes 65 and 66 are also provided in such a manner as to fill the respective openings 63a and 63b. Thus, the anode electrodes 65 are connected directly to the P^+-type doped semiconductor regions 51 through the respective openings 63a, while the cathode electrodes 66 are connected directly to the N^+-type highly-doped semiconductor regions 62 through the respective openings 63b.

[0066] The back illuminated photodiode array 3 further comprises a passivation film 71, a supporting film 72, filling electrodes 73a and 73b, UBMs 74a and 74b, and bumps 75a and 75b. The passivation film 71 is provided on the upper surface S1 of the N-type semiconductor substrate 50 in such a manner as to cover the insulating film 63, anode electrodes 65, and cathode electrodes 66. On the passivation film 71 is formed the supporting film 72. Also, the filling electrodes 73a and 73b penetrate through the passivation film 71 and the supporting film 72 to extend, respectively, from the anode electrodes 65 and the cathode electrodes 66 to the surface of the supporting film 72. On the exposed portions of the filling electrodes 73a and 73b at the surface of the supporting film 72 are formed the UBMs 74a and 74b. On the surfaces of the UBMs 74a and 74b on the opposite side of the filling electrodes 73a and 73b are formed the bumps 75a and 75b.

[0067] The effect of the back illuminated photodiode array 3 will here be described. In the back illuminated photodiode array 3, since there is provided the coating layer 53, the mechanical strength of the back illuminated photodiode array 3 is increased. Also, the increase in mechanical strength allows for dicing at a wafer level, whereby it is possible to obtain a chip-sized back illuminated photodiode array 3. Accordingly, there is achieved a back illuminated photodiode array 3 having a sufficiently small package.

[0068] Further, the coating layer 53 is arranged in such a manner that the portions provided on the recessed portions 52 are sunk lower than the portions provided on the outer edge portions 54 of the recessed portions 52. Therefore, even if a flat collet may be used in an assembling operation, the surface of the coating layer 53 provided on the recessed portions 52 is not brought into contact with the flat collet. Thus, the incident parts for to-be-detected light within the surface of the coating layer 53 cannot be damaged, whereby it is possible to suppress the scattering of to-be-detected light. Thus, a highly sensitive back illuminated photodiode array 3 is achieved.

[0069] There are also constructed a plurality of photodiodes by forming a plurality of P^+-type doped semiconductor regions 51 in a plurality of areas in the surface

layer on the upper surface S1 side of the N-type semiconductor substrate 50, and by forming recessed portions 52 in the rear surface S2 and in areas opposite the respective P+-type doped semiconductor regions 51. Therefore, the back illuminated photodiode array 3 can suitably be used for an image sensor, etc., in which each photodiode represents one pixel.

[0070] The back illuminated photodetector according to the present invention is not restricted to the above-described embodiments, and various modifications may be made. For example, in the back illuminated photodiode 1 shown in FIG. 1, a P-type semiconductor substrate may be used instead of the N-type semiconductor substrate 10. In this case, the doped semiconductor region 11 has N-type conductivity, while the highly-doped semiconductor layer 21 and the highly-doped semiconductor region 22 have P-type conductivity.

[0071] Although in FIG. 12 is shown an example of depositing a conductive material 33 made of Cu, Ni may be used instead of Cu to perform electroless plating of Ni directly on the surface of the anode electrodes 25 and the cathode electrodes 26 that are exposed from the openings 31a and 32a. In this case, it is possible to omit the step of polishing the surface of the conductive material 33 illustrated in FIG. 13.

[0072] Although in FIG. 15 an example of forming UBMs 34a and 34b as well as bumps 35a and 35b on the filling electrodes 33a and 33b is shown, there is also a method of employing the filling electrodes 33a and 33b themselves as bumps. That is, O_2, etc., is used to dry etch the surface of the supporting film 32 with the openings 32a being filled with the filling electrodes 33a and 33b (refer to FIG. 14). Thus, since the filling electrodes 33a and 33b partially protrude from the surface of the supporting film 32, the protruding portions can be used as bumps. In this case, it is also not necessary to form UBMs 34a and 34b. Alternatively, as a conductive material 33, a conductive resin may be used. This allows the operation of filling the through holes with electrodes by printing, etc., to be completed in a short time.

[0073] Also, in FIG. 19, as the semiconductor substrate 20, a bonded wafer in which an N+-type highly-doped semiconductor layer and an N-type doped semiconductor layer having an impurity concentration lower than that of the N+-type highly-doped semiconductor layer are bonded to each other may be used. In this case, the N-type doped semiconductor layer is to be provided on the upper surface S1 side, while the N+-type highly-doped semiconductor layer on the rear surface S2 side of the semiconductor substrate 20.

Industrial Applicability

[0074] In accordance with the present invention, it is possible to achieve a back illuminated back illuminated having a sufficiently small package as well as being capable of suppressing the scattering of to-be-detected light.

Claims

1. A back illuminated photodetector comprising:

   a first conductive type semiconductor substrate;
   a second conductive type doped semiconductor region provided in the first superficial surface layer of the semiconductor substrate;
   a recessed portion for incidence of to-be-detected light formed in the second surface of the semiconductor substrate and in an area opposite the doped semiconductor region; and
   a coating layer made of resin for transmitting the to-be-detected light, the coating layer being provided on the second surface,
   the coating layer being arranged in such a manner that the portion provided on the recessed portion in the second surface is sunk lower than the portion provided on the outer edge portion of the recessed portion.

2. The back illuminated photodetector according to Claim 1, further comprising a supporting film provided on the first surface of the semiconductor substrate to support the semiconductor substrate.

3. The back illuminated photodetector according to Claim 2, further comprising a filling electrode penetrating through the supporting film and connected electrically to the doped semiconductor region at one end thereof.

4. The back illuminated photodetector according to any one of Claims 1 to 3, wherein a highly-doped semiconductor region with impurities of the first conductive type added thereto at a high concentration is exposed across the entire side surface of the semiconductor substrate.

5. The back illuminated photodetector according to any one of Claims 1 to 4, wherein a highly-doped semiconductor layer with impurities of the first conductive type added thereto at a high concentration is provided in the bottom portion of the recessed portion within the second superficial surface layer of the semiconductor substrate.

6. The back illuminated photodetector according to any one of Claims 1 to 5, wherein a highly-doped semiconductor layer with impurities of the first conductive type added thereto at a high concentration is provided in the second superficial surface layer in the outer edge portion of the semiconductor substrate.

Fig.1

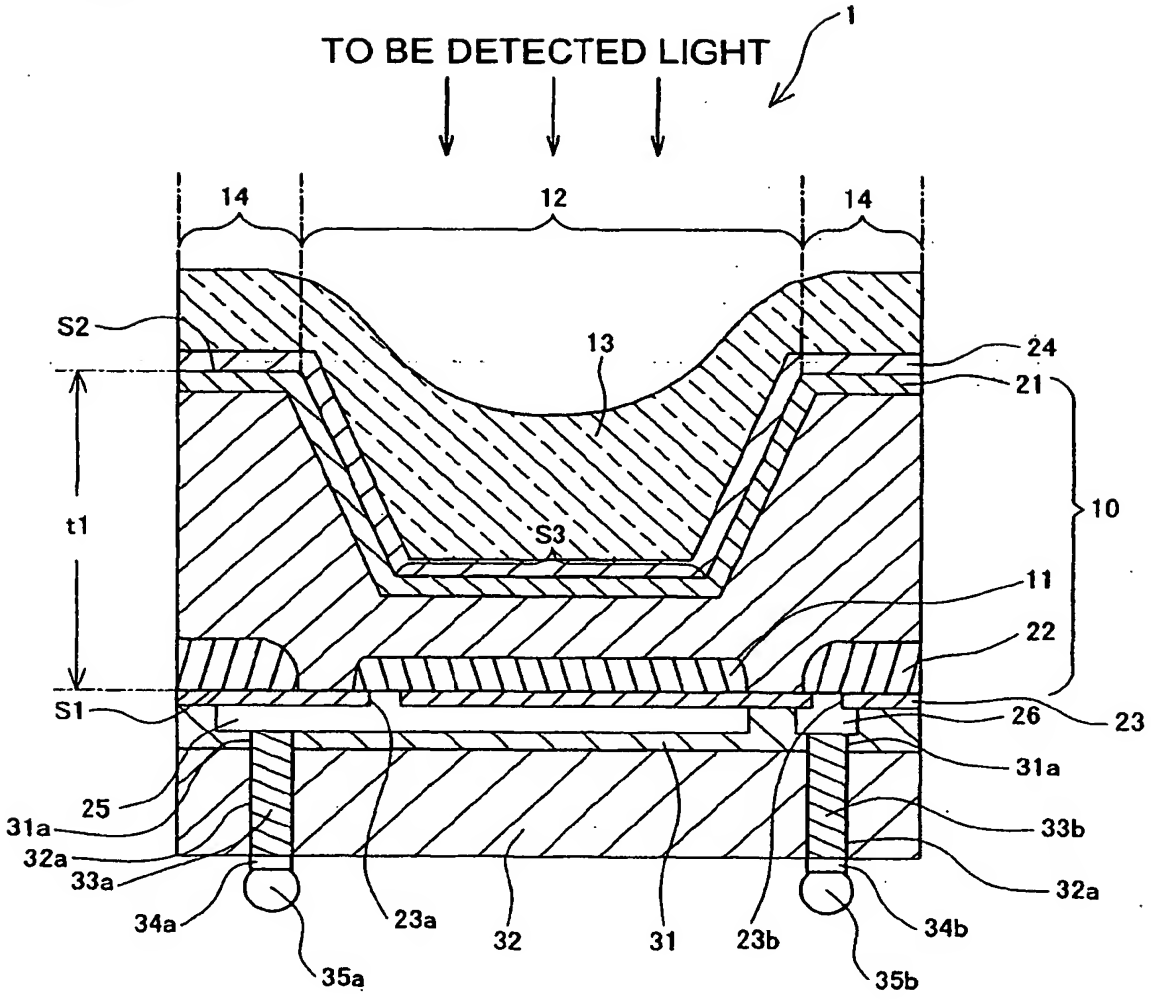
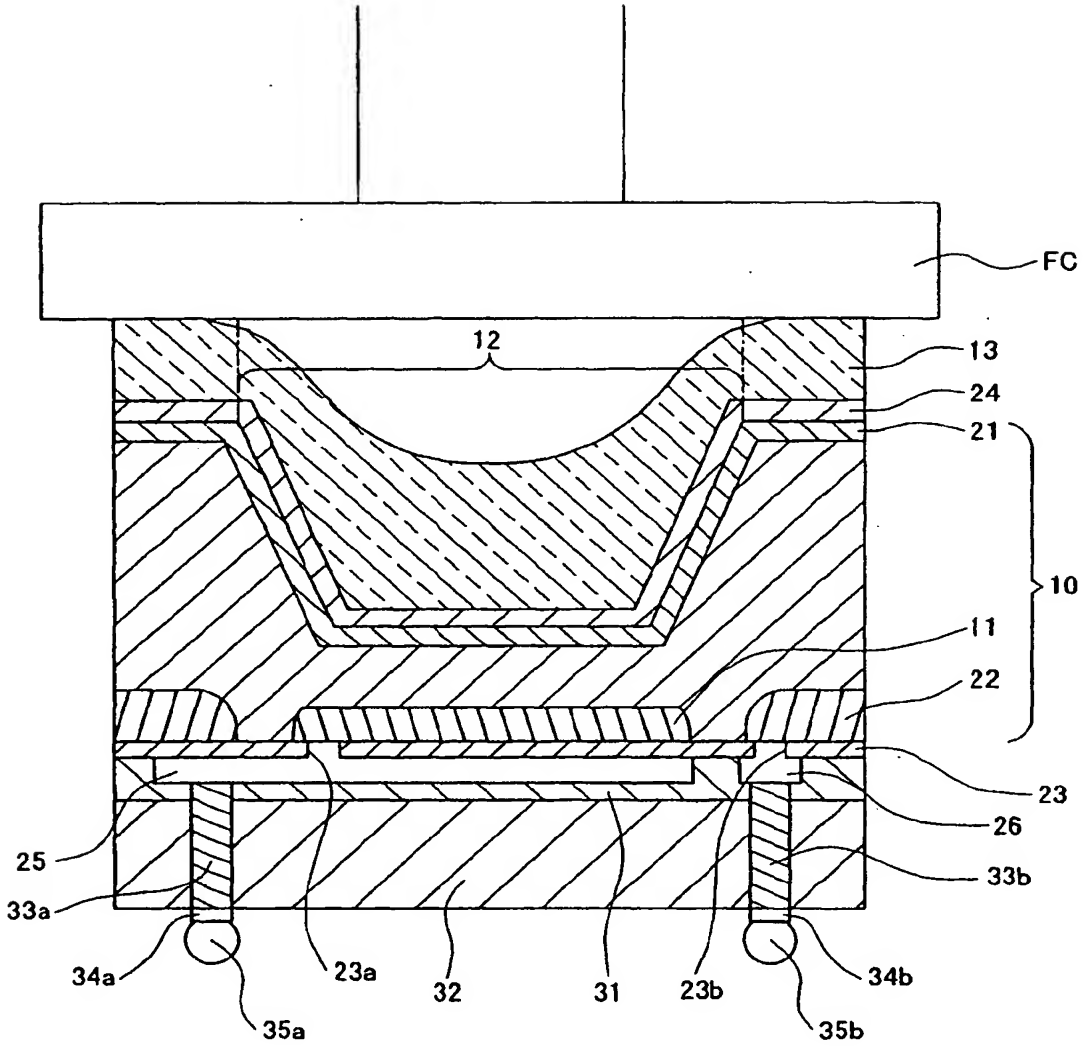


Fig.2


FC
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13
24
21
10
11
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33b
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32
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23b
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35a
35b

Fig.3

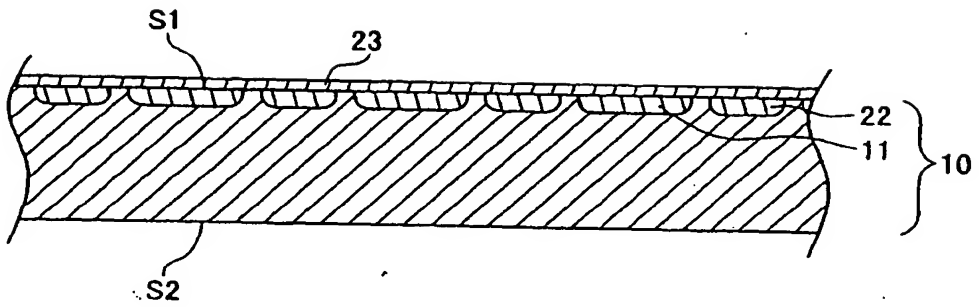


Fig.4

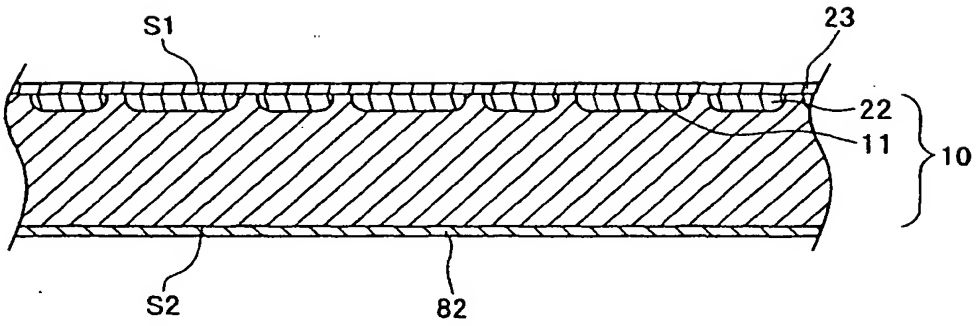


Fig.5

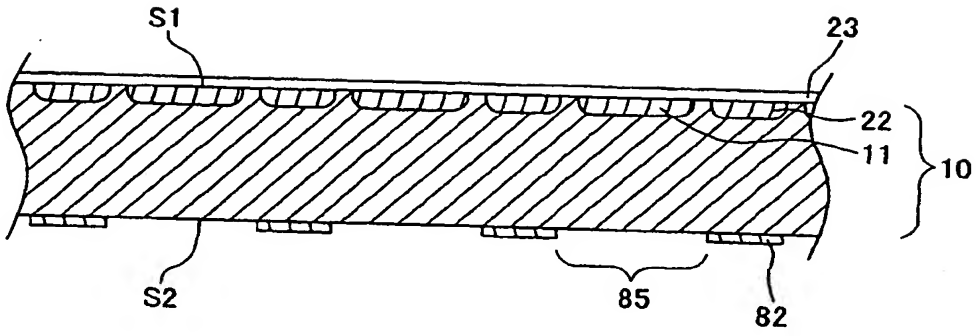


Fig.6

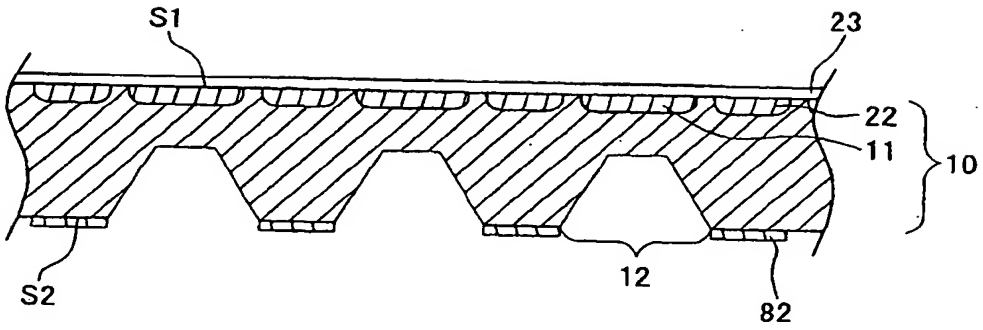


Fig.7

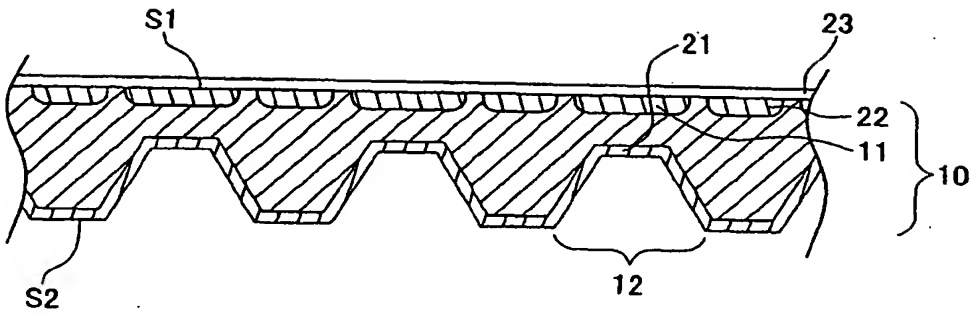


Fig.8

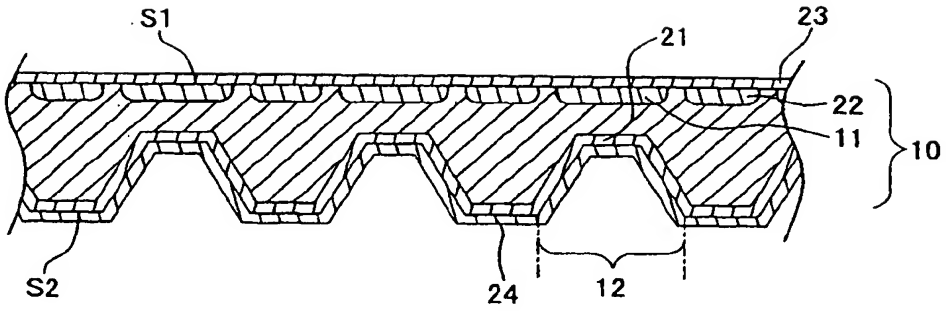


Fig.9

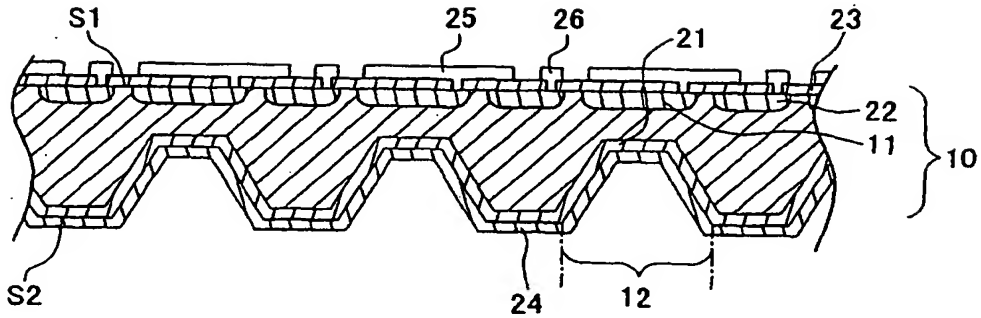


Fig.10

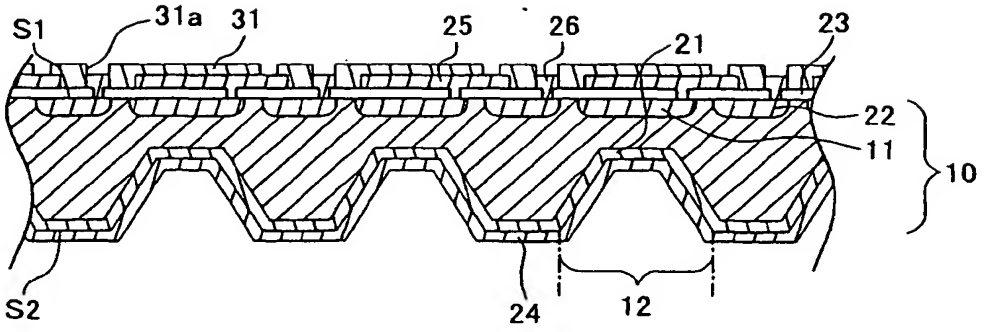


Fig.11

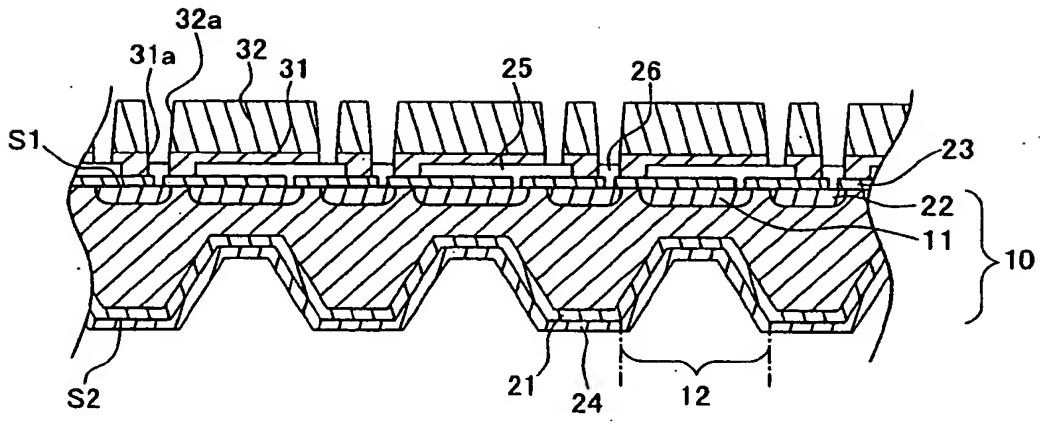


Fig.12

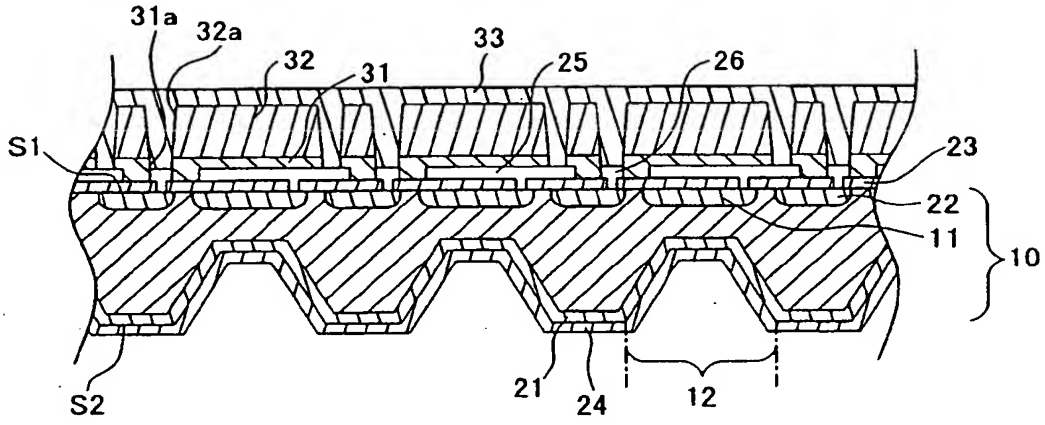


Fig.13

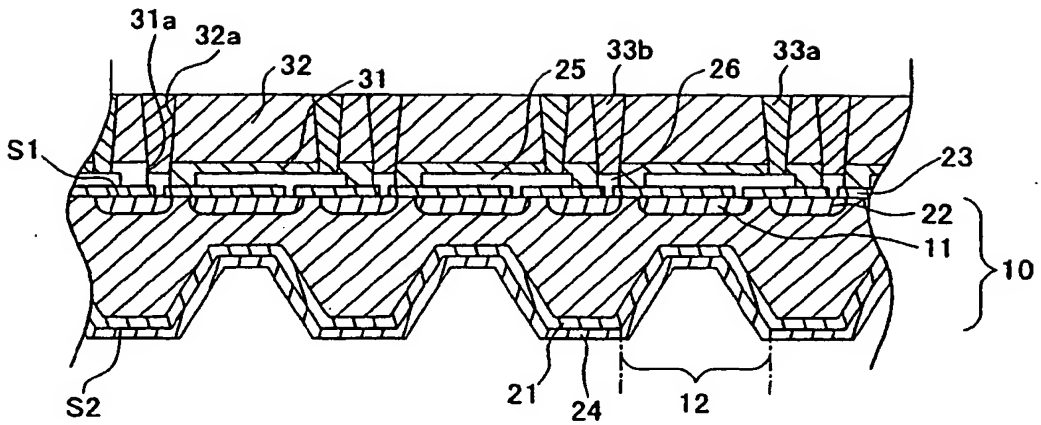


Fig.14

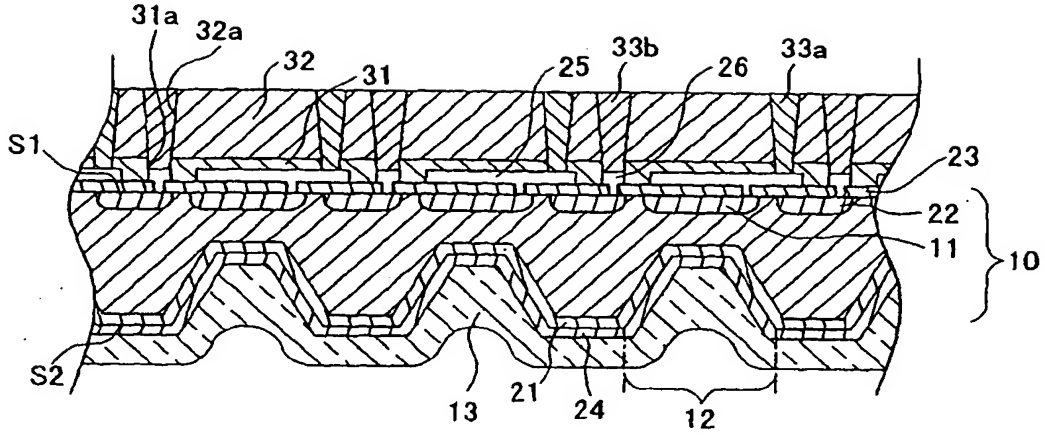


Fig.15

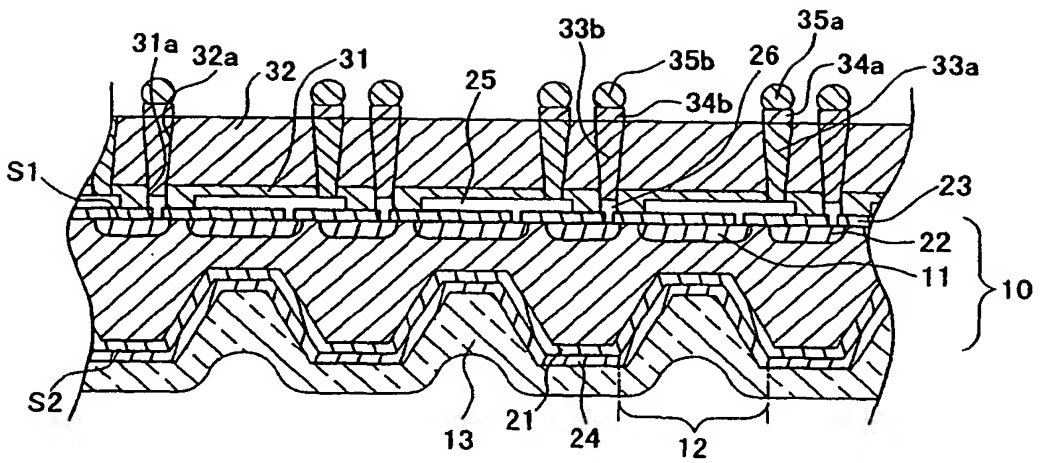
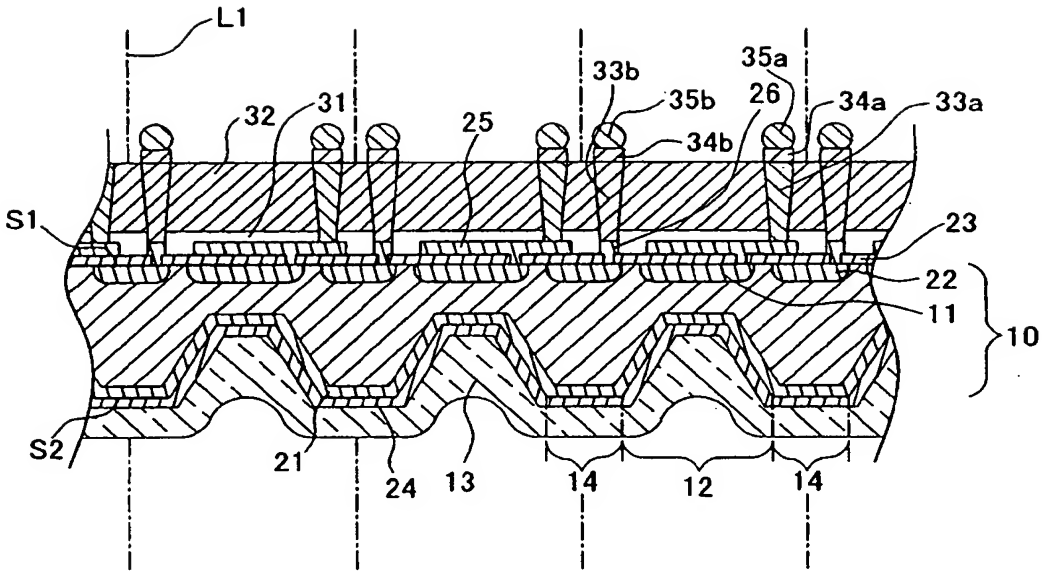


Fig.16


L1
33b
35a
35b
26
34a
33a
32
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34b
S1
23
22
11
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S2
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24
13
14
12
14

Fig.17

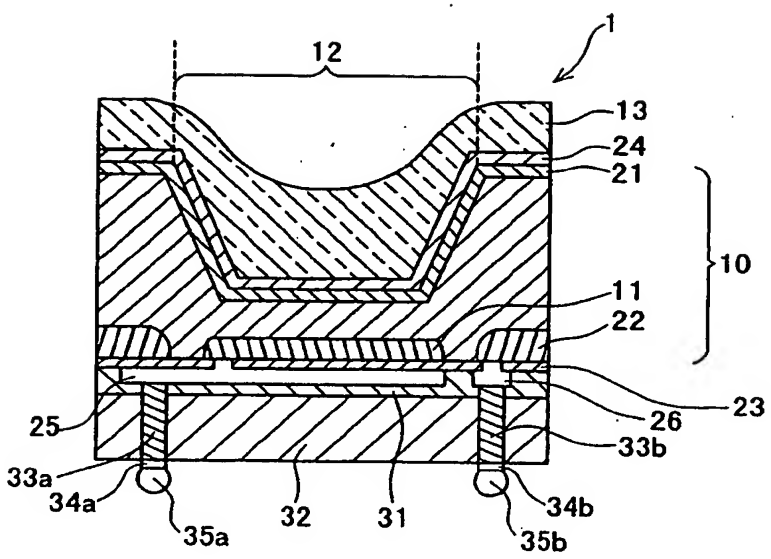
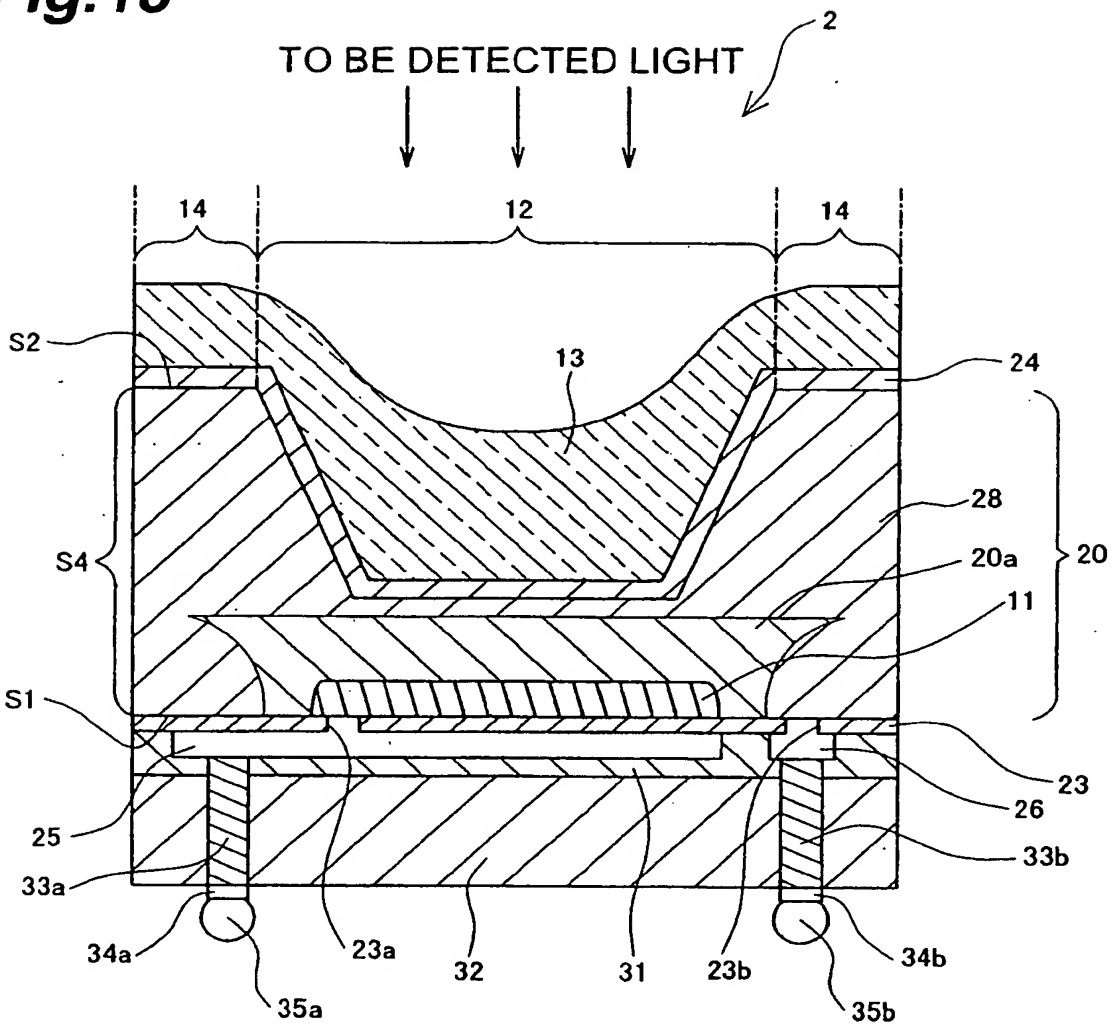


Fig.18


TO BE DETECTED LIGHT
2
14
12
14
S2
13
24
28
S4
20a
20
11
S1
23
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33b
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32
31
23b
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35a
35b

Fig.19

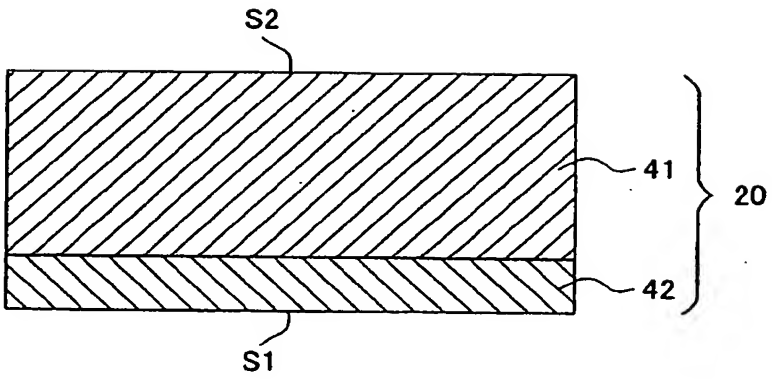


Fig.20

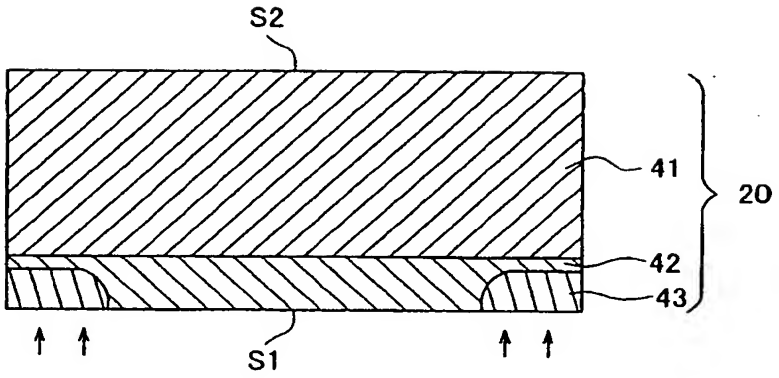


Fig.21

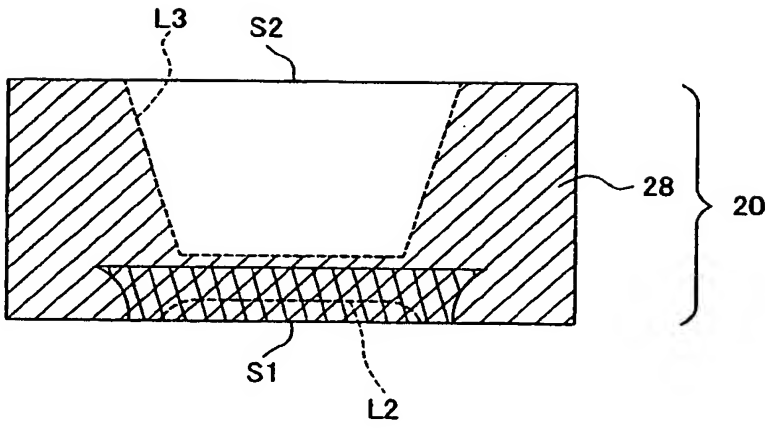


Fig.22

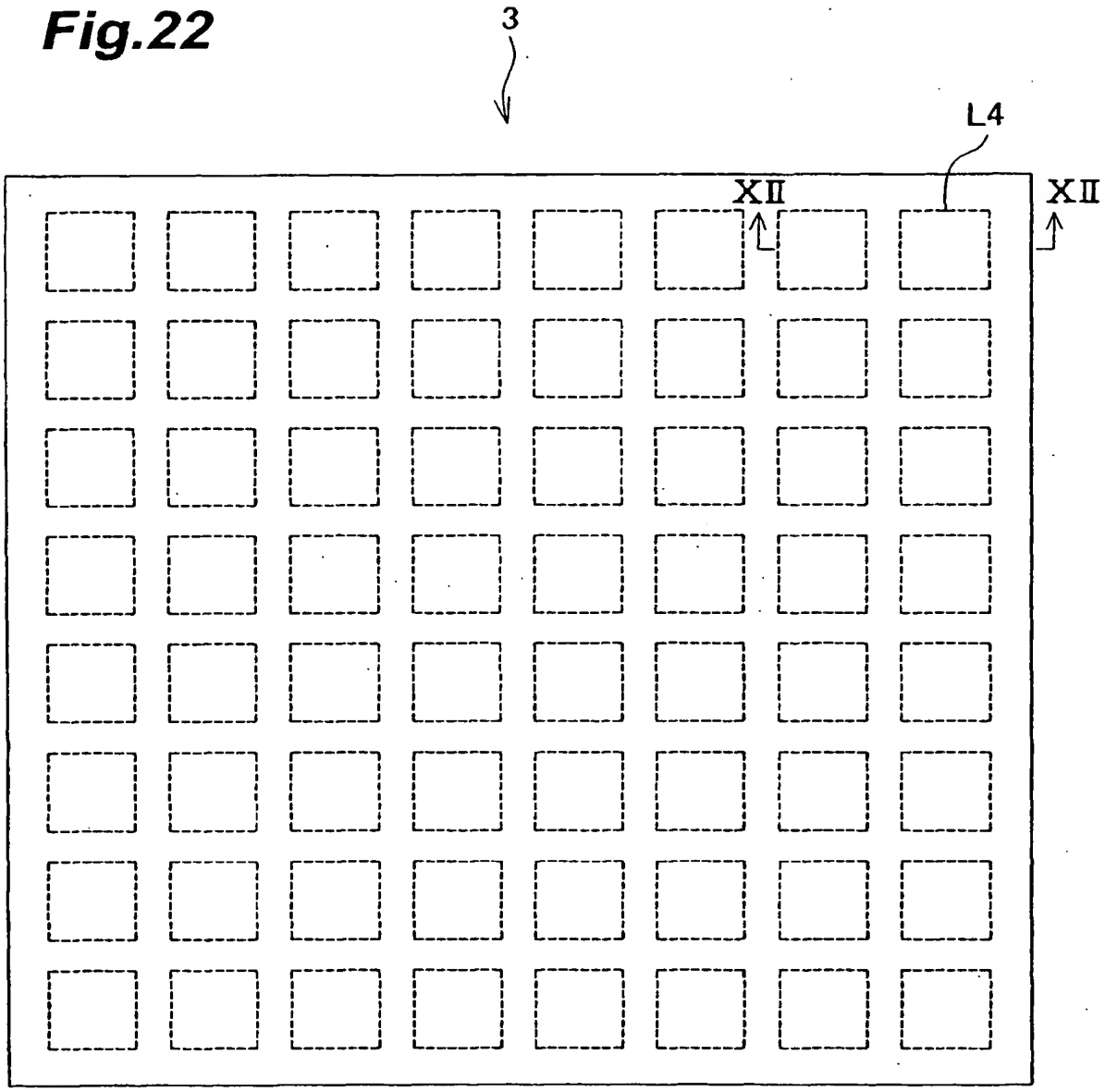


Fig.23

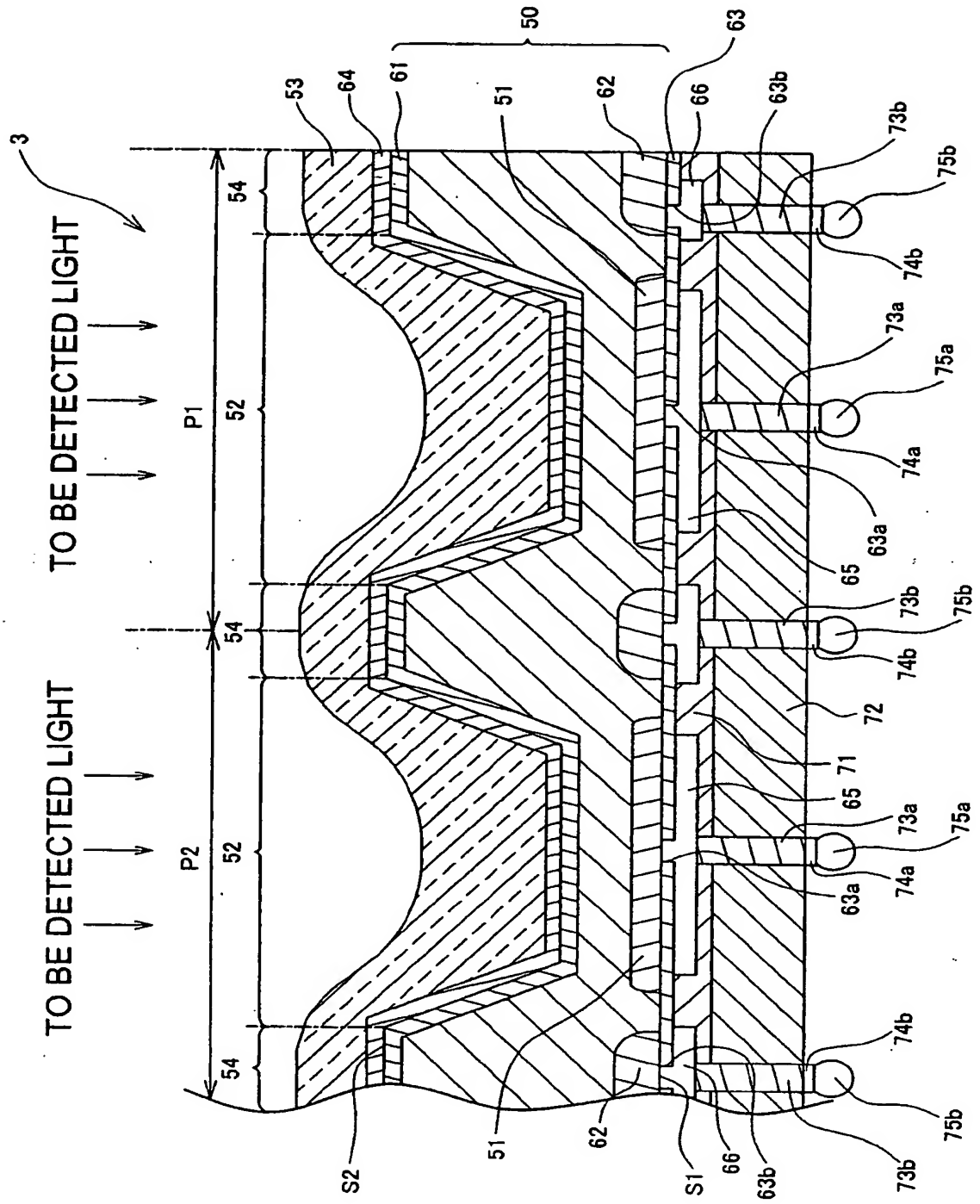
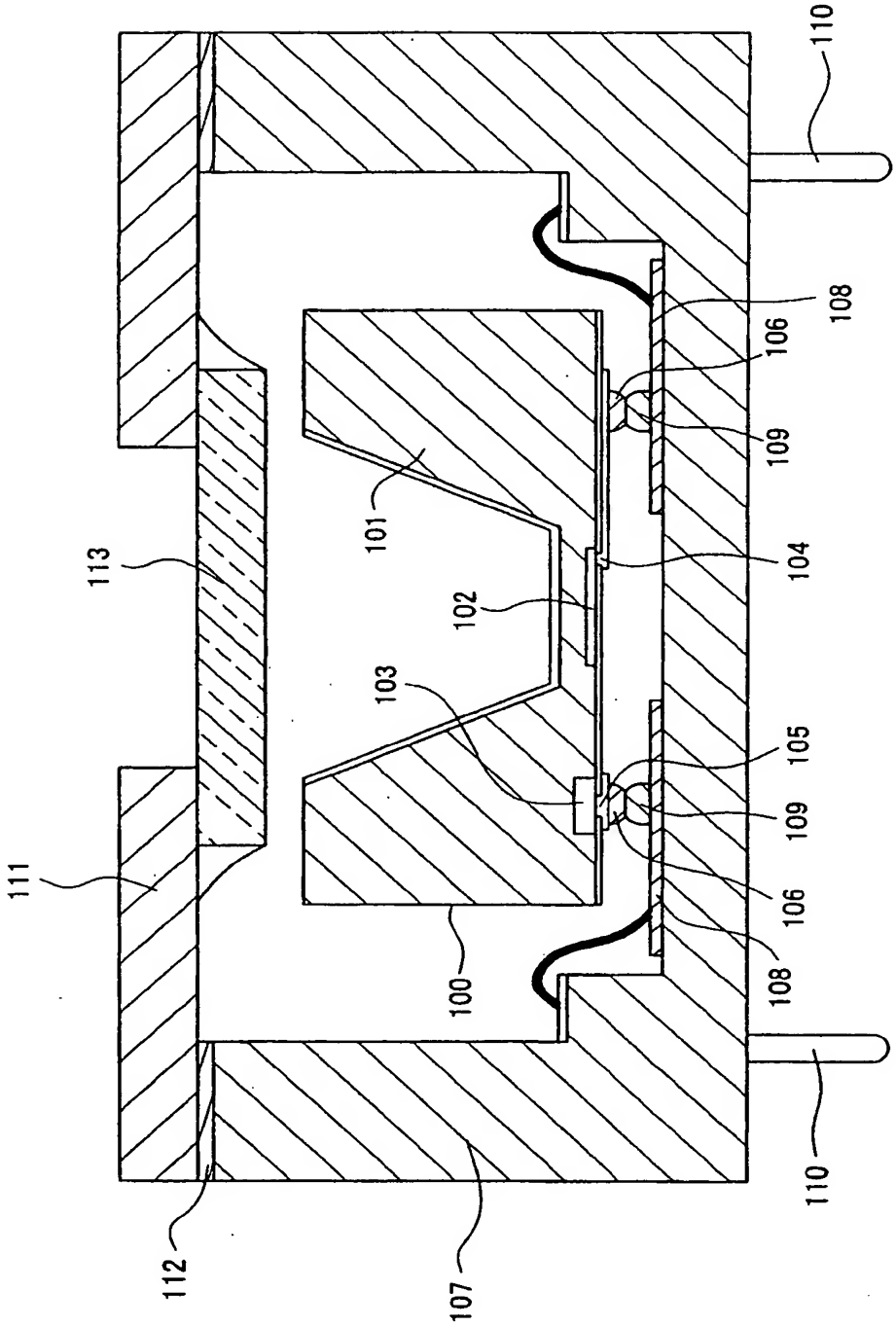


Fig.24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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/010410

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L31/10, H01L27/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L31/00-31/10, H01L27/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Toroku Jitsuyo Shinan Koho	1994-2004
Kokai Jitsuyo Shinan Koho	1971-2004	Jitsuyo Shinan Toroku Koho	1996-2004

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 96/36999 A1 (DR. JOHANNES HEIDENHAIN GMBH.), 09 May, 1996 (09.05.96), & EP 771475 A & DE 296023349 U & JP 10-508987 A & US 5852322 A1 Full text; all drawings	1-6
Y	JP 2000-299489 A (Hamamatsu Photonics Kabushiki Kaisha), 24 October, 2000 (24.10.00), Full text; all drawings	1-6
Y	Par. Nos. [0009] to [0011], [0018] to [0019]	4-6

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search 22 October, 2004 (22.10.04)	Date of mailing of the international search report 09 November, 2004 (09.11.04)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2004/010410

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2002-319669 A (Hamamatsu Photonics Kabushiki Kaisha), 31 October, 2002 (31.10.02), Figs. 1, 4 (Family: none)	2-6
X Y	JP 2-185070 A (Matsushita Electric Industrial Co., Ltd.), 19 July, 1990 (19.07.90), Full text; all drawings (Family: none)	1 2-6
A	WO 97/23897 A2 (DR. JOHANNES HEIDENHAIN GMBH.), 20 December, 1997 (20.12.97), & DE 19549228 A1 & EP 868751 A Fig. 5 & CN 1244949 A & JP 2000-502215 A & US 6175141 B1 & AT 233434 T	1-6

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